ABSTRACT OF THE DISCLOSURE

A multiport memory has a plurality of RAMs and a port expansion unit electrically connected to access ports of the RAMs. The port expansion unit includes an input circuit which allows access control information for activating the RAMs in parallel every memory cycles to be collectively inputted thereto by a plurality of memory cycles, a timing generator which generates internal clock signals capable of serially prescribing each memory cycle plural times during one cycle of a clock signal (ck), and a logic circuit capable of sequentially supplying the access control information inputted to the input circuit to the plurality of RAMs in parallel in parts every serial memory cycles synchronized with the internal clock signals. The port expansion unit allows access to the access ports with the plurality of RAMs as a single multiport memory apparently.